

B3  
cont

1 and thermally diffusing the p-type impurities and the semiconductor substrate 1. Then, a plurality of field insulating films 3 are formed on a principal surface of the p-type well 2 by selective oxidation so that the field insulating films 3 extend in parallel with one another, but perpendicularly to word lines which will be formed later. The field insulating films 3 are not illustrated in Fig. 8A, but are illustrated in Fig. 5.

On page 6, line 23, replace the paragraph as follows:

B4

In accordance with the above-mentioned method, when the first polysilicon layer 5a is etched, the thick field insulating films 3 exist below a region to be etched. When the second and first polysilicon layers 7a and 5a are patterned to thereby form the control gate 7 and the floating gate 5, a region where only a single polysilicon layer is etched is a region located above the field insulating regions 3. Hence, the above-mentioned undesirable recess 19 caused by etching a polysilicon layer is not formed. Accordingly, there is solved a problem that junction leakage occurs due to the recess, and resultingly data-writing and data-eliminating properties are deteriorated, and that a fabrication yield due to the breakage in a source region is reduced.

On page 13, line 12, replace the paragraph as follows:

B5

Then, a plurality of field insulating films 3 composed of silicon dioxide are formed in parallel by selective oxidation. The field insulating films 3 extend perpendicularly to word lines which will be formed later, and have a thickness in the range of 4000 to 8000 angstroms. The field insulating films 3 are not illustrated in Fig. 11A, but are illustrated in Fig. 10.

IN THE CLAIMS:

Please enter the following amended claims:

B6

21. (Amended) A method of fabricating an EEPROM semiconductor device, comprising the steps of: